Pin configuration for Dynamic Range Enhancement (DRE) Chip, Modified Multigain (MMG) architecture				
S.No.	**Pin Name**	**No. of pins needed**	**No. of pins that can be removed**	**Remarks**
1	Inputs: 1x and 4x	4	2	Need to see if 4x input pins are needed separately
2	Outputs: Samp out unbufferred	2		Direct output
3	Outputs: directly biffered	2		After single ended buffers at 2.5V.
4	Outputs: downconverted	2		Output from 2nd S/H, with NRZ output
5	1x and 4x outputs	4		
6	1.2V and 2.5V supply	4		2 pins for each supply
7	Ground	4		Same as supply pins count
8	Scan Chain	6	1	For digital logic control
9	Ibias 1x amp	2	1	
10	Ibias 4x amp	2	1	One each for diff pair and for CMFB
11	Ibias Samp amp	2	1	
12	Ibias buffers	2	1	Probably in 2.5V domain
13	DecisionBit, En4x_cont	2		
14	Reference Voltage	2		differential
15	Input offsets	2		
16	Comparator inputs	4		2 comparators, 4 inputs for differential comparison
17	Manual Overdrive, Gain Select	2		External input in case I decide to give a clock on this
18	Clock	2	1	Differential? (maybe not)
	Total	**50**	**8**	

Area estimate for single main chip				
S.No.	**Name**	**Area**		**Remarks**
1	Amplifier 1x	100ux100u		
2	Amplifier 4x	100ux100u		
3	Samp Amp	100ux100u		
4	R (Total of 6x1M, 12x200k)	300ux100u		
5	Cap (Total about 100pF) and some	600ux100u		
6	Buffer amplifiers (2 of them)	2*300ux100u		
7	Digital Circuits	200ux100u		
8	Comparators	2*100ux100u		
	Total Components area	2,500ux100u = 0.25 sqmm		
	Wiring etc.	Same as components area = 0.25sqmm		
	Total active area	**0.6 sqmm**		Preferably in dimension of 1.2mm x 0.5mm
	Area including pads	**1 sqmm**		Preferably 1.5mm x 0.7mm

Chips required and area estimate				
S.No.	**Name**	**Required area**	**Desired pin count/ min pin count**	**Remarks**
1	Only DRE, shared die with SAR	0.6 sqmm (active) (preferred 1.2 mm x 0.5 mm)	56 / 44	Pad area not included. This chip will be irradiated, along with SAR chip
2	Modified DRE, separate chip	1 sqmm (with pads)	56 / 44	Offset mechanism will be removed, transistor sizing will be adjusted accordingly. Evaluation of best performance that can be obtained with the proposed architecture. Will not be irradiated.
3	Combined DRE and SAR chip (?)	0.4 sqmm (active) (preferred 0.8mm x 0.5mm)	56 / 44 (conservative)	DRE output will be going into SAR chip. Not sure if this chip will be made or not (to be discussed in meetings)

Additional Notes	
1	Supplies used: 1.2V (main circuit), 2.5V (output buffers)
2	Devices used: 1.2V LVT, 2.5V RVT
3	Deep N-well devices not used currently (can we use them?)